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09/586,325	06/02/2000	Ulrich Bortfeld	02con360p	6473
25700	7590	11/28/2003	EXAMINER	
FARJAMI & FARJAMI LLP 16148 SAND CANYON IRVINE, CA 92618			CRAIG, DWIN M	
			ART UNIT	PAPER NUMBER
			2123	11
DATE MAILED: 11/28/2003				

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/586,325

Applicant(s)

BORTFELD ET AL.

Examiner

Dwin M Craig

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on <sup>10</sup>~~8-02-2000~~.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-14, 17-20, 23-31, 33 and 34 is/are rejected.
- 7) ☒ Claim(s) 9, 15, 16, 21, 22, 32 and 35 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

1. Claims 1-35 have been presented for reconsideration based on Applicant's amended claim language.

### Response to Arguments

2. Applicant's arguments filed on 10-2-2003 have been fully considered. Examiner's response is as follows.

2.1 Regarding Applicant's response to the rejection of Claim 1 under the Judicially Created Doctrine of Non-Statutory Double Patenting:

Applicants have argued:

The Examiner has rejected claim 1 under the judicially created doctrine of double patenting as being unpatentable over claim 1 of U.S. Application Serial No. 09/586,433.

Along with the present amendment, Applicant has submitted a terminal disclaimer to overcome the Examiner's rejection under the judicially created doctrine of double patenting with respect to claim 1 of U.S. Application Serial No. 09/586,433. Applicant respectfully submits that the enclosed terminal disclaimer overcomes the Examiner's double patenting rejection.

The Examiner thanks the Applicant for sending in the terminal disclaimer, *see paper number 10*, and withdraws the earlier rejection of Claim 1 based on the Judicially Created Doctrine of Non-Statutory Double Patenting.

2.2 Regarding the Applicants response to the Examiner's objection to the specification for improper incorporation by reference of Application 09/586,433:

Applicants have argued that:

The Examiner has indicated that the incorporation by reference on page 1 of the present application is improper. Applicant has amended the paragraph beginning on page 1, line 6 to further specify the Serial Number and filing date of the U.S. Application which is incorporated in its entirety by

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reference. Applicant respectfully submits that the incorporation by reference on page 1 of the present application now meets the requirements of MPEP §608.01(p).

The Examiner asserts that the Applicant has overcome the objection to the specification by adding the correct serial number of the incorporated application and the Examiner withdraws the earlier objection to the specification for improper incorporation by reference.

**2.3**     Regarding the Applicants response to the 35 U.S.C. 101 Utility rejection of claims 17-22 and 33-35:

Applicants have argued that:

The Examiner has rejected claims 17-22 and 33-35 under 35 USC §101 as being directed to non-statutory subject matter. Applicant has amended independent claims 17 and 33 to specify a "computer program product embodied on a computer-readable medium, which when executed, causes a processing system to simulate a system design." Applicant respectfully submits that independent claim 17, and its corresponding dependent claims 18-22, and independent claim 33, and its corresponding dependent claims 34-35, now meet the requirements of 35 USC §101.

The Examiner asserts that the amended claim language to independent Claims 17 and 33 have overcome the earlier 35 U.S.C. 101 Utility rejections of independent Claims 17 and 33 and the Examiner withdraws the rejection of Claims 17-22 and 33-35 under the 35 U.S.C. 101 Utility requirement.

**2.4**     Regarding the Applicants response to the 35 U.S.C. 102 rejections of Claims 1, 5, 6, 10, 17, 23, 24, 28, 29, 33 and 34:

Applicants have argued:

The Examiner has rejected claims 1, 5, 6, 10, 17, 23, 24, 28, 29, 33 and 34 under 35 USC §102(a) as being anticipated by Hollander (USPN 6,182,258) ("Hollander `258"). Applicant respectfully disagrees; however, in order to expedite the prosecution of the present application, applicant has amended independent claims 1, 10, 17, 23 and 33. For the reasons that follow, applicant respectfully submits that claims 1-35 are patentably distinguishable over Hollander `258.

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As amended, claims 1, 10, 17, 23 and 33 specify, among other things, a computer implemented method and/or instructions for simulating a system design, including at least one function call comprising "a cycle-based function corresponding to a collection of communication events." As discussed in the present application, "the events that, comprise frequently repeated communications maybe condensed into a single function call. A collection of related function calls may be referred to as an interface." Page 22, lines 13-15 of the present application. With this arrangement, detailed saturated event driven simulation can be avoided, and the invention advantageously achieves cycle accurate simulations with significantly improved simulation speed.

In contrast, Hollander `258 fails to disclose or suggest such an approach. Rather, Hollander `258 is directed to an improved test bench apparatus and method. To clarify, Hollander `258 is not directed to a method for simulating a system, as specified by claim 1, 10, 17, 23 and 33. Instead, Hollander `258 is directed to a technique for generating system tools used to verify a device under test ("DUT"). See, for example, col. 4, lines 44-52 of Hollander `258. The DUT may be a module, chip, simulation and/or system, and Hollander `258 discloses a testbench, which can be used, and re-used to test the DUT. Specifically, Hollander `258 discloses a technique for generating test vectors used as input stimuli to, for example, a simulator. However, Hollander `258 is not directed to the system simulator itself, nor to a method for simulating a system, as specified by claims 1, 10, 17, 23 and 33. As such, Hollander `258 neither discloses nor remotely suggests the computer implemented method and/or instructions for simulating a system design, as specified by claims 1, 10, 17, 23 and 33. In sum, Hollander '258 is simply directed to a tool for generating a test bench suitable for testing system simulations.

The Examiner asserts that a reasonable interpretation of Applicants claim language does not limit the Applicant to a "system" instead the claim language is directed towards a system design containing at least two components. The Examiner asserts that the *Hollander* reference, *U.S. Patent 6,182,258*, does teach a method of simulating a system design containing at least two components (**Figure 5 Item 172 "HARDWARE MODEL", Col. 6 Lines 33-67**), specifically, *"The unified system interface can also be adapted for custom modeling environment. In addition, the invention is readily linked with existing code or models such as in C, C++, Verilog and VHDL languages."* and *"For Example, the invention can be used to test a device under testing (DUT) such as modules, chips, simulations, and application specific integrated circuits (ASICs'), as well as complete systems, including systems having embedded logic. The invention*

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is also operable with cycle-based and event-driven simulation environments." The Examiner asserts that *complete systems* is a system with more than one component and at least two components and the *simulations and cycle-based simulation environments* teaches the limitations disclosed in the preamble of Applicants claim language.

Moreover, as discussed above, claims 1, 10, 17, 23 and 33 have been amended to specify at least one "function calls comprising a cycle-based function corresponding to a collection of communication events." Such an approach is neither disclosed nor suggested by Hollander '258. For these reasons, applicant respectfully submits that the rejection of independent claims 1, 10, 17, 23 and 33, and their corresponding dependent claims 2-9, 11-16, 18-22, 24-32 and 34-35 has been traversed, and that, therefore, claims 1-35 should now be allowed.

The Examiner asserts that Applicant's arguments are persuasive in that the Hollander reference does not teach the amended limitations in the new claim language and over comes the 35 U.S.C. 102 rejections of claims 1, 5, 6, 10, 17, 23, 24, 28, 29, 33 and 34. The Examiner withdraws the 35 U.S.C. 102 rejections of claims 1, 5, 6, 10, 17, 23, 24, 28, 29, 33 and 34.

**2.5** Regarding the Applicants response to the 35 U.S.C. 103 rejections of Claims 1, 10, 17, 23 and 33 under 35 U.S.C. 103:

Applicants have argued:

The Examiner has further rejected claims 1, 10, 17, 23 and 33 under 35 USC §103(a) as being unpatentable over Bargh, et al. (USPN 6,195,627) ("Bargh, '627") in view of Roy, et al. (USPN 6,295,517) ("Roy '517"). Applicant respectfully disagrees; however, in order to expedite the prosecution of the present application, applicant has amended independent claims 1, 10, 17, 23 and 33, as discussed above. For the reasons that follow, applicant respectfully submits that claims 1-35 are patentably distinguishable over the cited references, considered singly or in combination.

As acknowledged by the Examiner, Bargh '627 fails to disclose or suggest "identifying components and generating cycle accurate information." Page 5 of the Detailed Action. The Examiner, however, cites Roy '517, and, specifically, Figures 5A, 513, col. 3, lines 6-11, col. 6, lines 1-14, col. 8, lines 10-48, col. 12, lines 61-67 and col. 13, lines 1-13 of Roy '517. stating that the clustering technique of Roy '517 could be combined with Bargh '627 to achieve the present invention as defined by claims 1, 10, 17, 23 and 33. Applicant respectfully disagrees that the combined disclosures of

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Bargh `627 and Roy `517 would result in present invention as defined by claims 1, 10, 17, 23 and 33.

With specific reference to Roy `517, Roy `517 discloses a cluster-based simulation architecture and method employing event-triggered cycle-based simulation or oblivious triggered cycle-based simulation. The disclosure of Roy `517 makes clear that the technique disclosed in Roy `517 "is addressed to RTL simulation." Col. 5, line 15 of Roy `517. That is, Roy `517 is a technique for simulation at the register transfer level ("RTL"), which is at a substantially lower level of abstraction than the behavioral level corresponding to the cycle-based simulation method specified by claims 1, 10, 17, 23 and 33. See, for example, Figure 1 of the present application. Thus, while the disclosure of Roy `517 employs the use of event-triggered cycle-based simulation or oblivious triggered cycle-based simulation, such techniques are applicable for generating RTL simulations systems, not behavioral level simulation systems.

Moreover, Roy `517 also points out that "the circuit designer, however, may require that certain portions of the Circuit Description 101 be simulated at higher or lower levels of modeling abstraction. Such portions are separated out by Front-end/Network Creation 102 and converted into an alternative conventional circuit representation suitable for conventional simulation techniques." Col. 5, lines 15-21 of Roy `517. Thus, according to Roy `517, its teachings are not applicable to simulation systems at a "higher" level of modeling abstraction, including the behavioral level. Instead conventional systems are employed for simulations at levels other than RTL.

Furthermore, as discussed above, claims 1, 10, 17, 23 and 33 have been amended to specify at least one function call comprising "a cycle-based function corresponding to a collection of communication events." Such an approach is neither disclosed nor suggested by Bargh `627 and Roy `517. For these reasons, applicant respectfully submits that the rejection of independent claims 1, 10, 17, 23 and 33 has been traversed, and that, therefore, independent claims 1, 10, 17, 23 and 33, and their corresponding dependent claims 2-9, 11-16, 18-22, 24-32 and 34-35 should now be allowed.

The Examiner asserts that Applicants arguments are persuasive in regards to the 35 U.S.C. 103 rejections of Claims 1, 10, 17, 23 and 33 by Bargh et al. U.S. Patent 6,195,627 in view of Roy et al. U.S. Patent 6,295,517 and withdraws the earlier 35 U.S.C. 103 rejections of these claims.

**2.6** Regarding Applicants response to the 35 U.S.C. 103 rejections of Claims 2-4, 7, 8, 11-14, 18-20, 25-27, 30 and 31:

Applicants have argued that:

The Examiner has further rejected dependent claims 2-4, 7, 8, 11-14, 18-20, 25-27, 30 and 31 under 35 USC §103(a) as being unpatentable over Hollander `258 in view of Malin, et al. (USPN 5,732,192) ("Malin `192"). As

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discussed above, independent claims 1, 10, 17 and 23 are patentably distinguishable over Hollander `258 and, as such, claims 2-4, 7 and 8 depending from independent claim 1, claims 11-14 depending from independent claim 10, claims 18-20 depending from independent claim 17, and claims 25-27, 30 and 31 depending from independent claim 23 are, a fortiori, also patentably distinguishable over Hollander `258. Accordingly, claims 4-10 and 24-26 are patentably distinguishable over Hollander `258 in view of Malin `192.

The Examiner asserts that Applicants arguments are persuasive in regards to the *Hollander* reference as cited above in paragraph 2.4 above and withdraws the 35 U.S.C. 103 rejections of Claims 2-4, 7, 8, 11-14, 28-20, 25-27, 30 and 31.

An updated search has revealed new art.

**Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.



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3. **Claims 1, 5, 6, 10, 17, 23, 24, 28, 29, 33 and 34** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hollander U.S. Patent 6,182,258** in view of **Chan U.S. Patent 6,466,898**.

3.1 As regards independent **Claims 1, 10, 17, 23 and 33** the *Hollander* reference discloses a simulation environment with more than one model (**Figures 1-8, Col. 2 Lines 50-67, Col. 3 Lines 1-3, Col. 4 Lines 58-65**), using a high-level programming language (**Col. 1 Lines 55-61, Col. 3 Lines 18-28, Col. 4 Lines 52-58, Col. 6 Lines 40-45, Col. 7 Lines 1-11**), where cycle accurate information is generated (**Figure 6 Item 86, Col. 3 Lines 18-28, Col. 10 Lines 24-28**).

However, the *Hollander* reference does not expressly disclose *at least one of said function calls comprises a cycle-based function corresponding to a collection of communications events*:

*Hollander* discloses that there is a need in the art for the reduction of verification time (**Hollander Col. 2 Lines 8-9**).

An ordinary artisan would have been motivated to search the system simulation art for a method of reducing the verification time of simulated systems, as suggested by the *Hollander* reference in order to overcome the express deficiencies of the reference in regards to the need for a function call that comprises a cycle-based function corresponding to a collection of communications events in order to reduce the time needed to model and/or verify a simulated design. In the related art of Event driven simulation the *Chan* reference discloses a function call that comprises a cycle-based function corresponding to a collection of communications events (**Figure 4, 8, 11, 12, 15, 16, 19, 21, Col. 6 Lines 15-24, Col. 7 Lines 8-45, Col. 13 Lines 44-60**).

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Thus, it would have been obvious, to one of ordinary skill in the art, at the time of the invention was made, to have modified the simulation and verification models of the *Hollander* reference with the function calls that comprises a cycle-based function corresponding to a collection of communications events of the *Chan* reference since there is a need for a general-purpose multithreaded logic simulator that supports both VHDL and Verilog languages in a single program to perform both a event-driven and a cycle-based logic simulation on a multiprocessor platform chosen by the user (**Chan Col. 3 Lines 9-16**).

**3.2** As regards dependent **Claims 5, 6 and 29** the *Hollander* reference discloses clock and signal functions (**Figures 4, 6, Col. 18 Lines 38-45**).

**3.3** As regards dependent **Claims 24, 28 and 34** the *Hollander* reference discloses using a high level programming language (**Col. 1 Lines 55-61, Col. 3 Lines 18-28, Col. 4 Lines 52-58, Col. 6 Lines 40-45, Col. 7 Lines 1-11**).

**4.** **Claims 2-4, 7, 8, 11-14, 18-20, 25-27, 30 and 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hollander U.S. Patent 6,182,258** in view of **Chan U.S. Patent 6,466,898** and in further view of **Malin et al U.S. Patent 5,732,192**.

**4.1** As regards independent **Claims 1, 10, 17, 23 and 33** see paragraph **3.1** above.

**4.2** As regards dependent **Claims 2-4, 7, 8, 11-14, 18-20, 25-27, 30 and 31** the *Hollander* reference does not expressly disclose a component management system.

The *Malin et al.* reference discloses a component management system for simulation (**Figures 1A-17**).

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It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Hollander* reference with the *Malin et al.* reference because (*motivation to combine*) the *Malin et al.* reference discloses a flexible method of generating global models that provide ease of simulation without having to have specific information about the systems being modeled and abstracted (*Malin et al. Col. 2 Lines 43-51*).

**Allowable Subject Matter**

5. Claims 9, 15, 16, 21, 22, 32 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and once all other rejections/objections have been traversed.

**Conclusion**

6. Claims 1-35 have been presented for reconsideration in view of the amended claim language. Claims 1-8, 10-14, 17-20, 23-31, 33 and 34 are rejected. Claims 9, 15, 16, 21, 22, 32 and 35 are objected to.

6.1 Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

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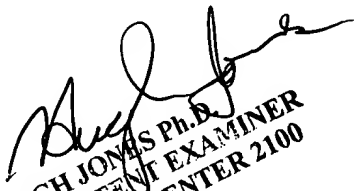
the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**6.2** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC  
November 20, 2003

  
HUGH JONES Ph.D.  
PRIMARY PATENT EXAMINER  
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